IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Kahle et al.	§	
	§	
Serial Number: 10/645,024	§	
	§	Group Art Unit: 2115
Filed: August 21, 2003	§	
	§	
For: POWER THROTTLING METHOD AND APPARATUS	§	Examiner: Dennis M. Butler
	§	

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

RESPONSE

Dear Sir:

In response to the Restriction Action dated June 14, 2006 ("Restriction Action"), Applicants respond as follows:

CLAIMS

1-15. (Cancelled)

16. (New) A method of conserving power in a computer processor, comprising:

reading a software-accessible control register;

determining an idle status of a subunit of the computer processor based on the control register;

providing a clock signal to the subunit based on the determined idle status; and

providing a power voltage to the subunit based on the determined idle status.

17. (New) The method as recited in Claim 16, wherein the control register comprises a plurality of architected bits in a machine state register and at least one bit of the plurality of architected bits is associated with at least one subunit of the computer processor.

18. (New) The method as recited in Claim 17, wherein determining the idle status comprises reading the at least one bit associated with the at least one subunit of the computer processor.

19. (New) The method as recited in Claim 16, further comprising setting one or more of a plurality of bits in the control register based on an idle status of a subunit of the computer processor.

20. (New) The method as recited in Claim 16, wherein the computer processor comprises data flow circuitry comprising a plurality of data flow sections, at least one data flow section configured as a subunit of the computer processor.

21. (New) The method as recited in Claim 16, wherein the computer processor comprises upper and lower bit data register circuitry portions, at least the upper bit data register circuitry portion configured as a subunit of the computer processor.

22. (New) The method as recited in Claim 16, wherein:

the computer processor comprises partitioned dataflow registers comprising a lower portion register consistent in size with the lowest instruction width software to be used in the computer processor; and

the control register comprises an architected control register bit indicating the width of the greatest instruction width presently being used by the computer processor.

23. (New) The method as recited in Claim 16, wherein the computer processor comprises partitioned arithmetic logic units (ALUs), comprising an upper ALU and a lower ALU, at least the upper ALU configured as a subunit of the computer processor.

24. (New) The method as recited in Claim 16, wherein the computer processor comprises a floating point logic unit (FPU), the FPU configured as a subunit of the computer processor.

25. (New) An apparatus for conserving power in a computer processor, comprising:

a software accessible control register having predetermined bit positions indicating subunits of the computer processor;

a local clock buffer coupled to the control register and configured to provide a clock signal to the subunit based on the predetermined bit position associated with the subunit; and

a voltage signal coupled to the control register and configured to provide a power voltage to the subunit based on the predetermined bit position associated with the subunit.

26. (New) The apparatus as recited in Claim 25, wherein the control register comprises a plurality of architected bits in a machine state register and at least one bit of the plurality of architected bits is associated with at least one subunit of the computer processor.

27. (New) The apparatus as recited in Claim 25, further comprising software configured to set one or more of the predetermined bit positions based on an idle status of a subunit of the computer processor.

28. (New) The apparatus as recited in Claim 25, wherein the computer processor comprises data flow circuitry comprising a plurality of data flow sections, at least one data flow section configured as a subunit of the computer processor.

29. (New) The apparatus as recited in Claim 25, wherein the computer processor comprises upper and lower bit data register circuitry portions, at least the upper bit data register circuitry portion configured as a subunit of the computer processor.

30. (New) The apparatus as recited in Claim 25, wherein:

the computer processor comprises partitioned dataflow registers comprising a lower portion register consistent in size with the lowest instruction width software to be used in the computer processor; and

the control register comprises an architected control register bit indicating the width of the greatest instruction width presently being used by the computer processor.

31. (New) The apparatus as recited in Claim 25, wherein the computer processor comprises partitioned arithmetic logic units (ALUs), comprising an upper ALU and a lower ALU, at least the upper ALU configured as a subunit of the computer processor.

32. (New) The apparatus as recited in Claim 25, wherein the computer processor comprises a floating point logic unit (FPU), the FPU configured as a subunit of the computer processor.

33. (New) A computer program product for conserving power in a computer processor, the computer program product having a medium with a computer program embodied thereon, the computer program comprising:

computer program code for reading a software-accessible control register;

computer program code for determining an idle status of a subunit of the computer processor based on the control register;

computer program code for providing a clock signal to the subunit based on the determined idle status; and

computer program code for providing a power voltage to the subunit based on the determined idle status.

34. (New) The computer program product as recited in Claim 33, wherein the control register comprises a plurality of architected bits in a machine state register and at least one bit of the plurality of architected bits is associated with at least one subunit of the computer processor.

35. (New) The computer program product as recited in Claim 34, wherein computer program code for determining the idle status comprises computer program code for reading the at least one bit associated with the at least one subunit of the computer processor.

36. (New) The computer program product as recited in Claim 33, further comprising computer program code for setting one or more of a plurality of bits in the control register based on an idle status of a subunit of the computer processor.

REMARKS

The Restriction Action dated June 14, 2006 has been carefully considered. Claims 16-36 are pending. Claims 1-15 have been cancelled in this Response. Claims 16-36 are new and are added in this Response. Reconsideration and allowance are respectfully requested in light of the above amendments and following remarks.

Claims 1-15 stand restricted under 35 U.S.C. § 121, Manual of Patent Examining Procedure (MPEP) §§ 806.05(d). In an earlier action, dated March 9, 2006, the Examiner identified seven groups of Claims: Group I (Claims 1, 3, 4), Group II (Claims 2, 13), Group III (Claim 5), Group IV (Claims 6, 9, 14), Group V (Claims 7, 9, 15), Group VI (Claims 8, 9), and Group VII (Claims 10, 11, 12). Applicants respectfully traverse the Examiner's characterization of the Claims and the restriction requirement based thereon.

In the current Restriction Requirement, the Examiner advises Applicants to provide a Response that includes "an election of species or invention to be examined even though the requirement be traversed" and "identification of the claims encompassing the elected invention." Restriction Action, at Page 2. Accordingly, Applicants elect, with traverse, the Examiner's identified Group IV (Claims 6, 9, and 14).

Applicants respectfully resubmit new Claims 16-36 in this Response. Support for Claims 16-36 can be found, among other places, at Page 6, line 4, through Page 9, line 9 of the original Application. Applicants respectfully submit that new Claims 16-36 generally encompass the elected invention. Moreover, Applicants respectfully submit that new Claims 16-36 limit prosecution of the present Application to a single elected invention and that entering new Claims 16-36 will significantly advance prosecution of this Application. Accordingly, Applicants respectfully request that Claims 16-36 be entered and fully allowed.

Applicants do not believe that any fees are due; however, in the event that any fees are due, the Commissioner is hereby authorized to charge any required fees due (other than issue fees), and to credit any overpayment made, in connection with the filing of this paper to Deposit Account No. 50-0605 of CARR LLP.

Should the Examiner require any further clarification to place this Application in condition for allowance, the Examiner is invited to telephone the undersigned at the number listed below.

Respectfully submitted,

CARR LLP

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